AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-18 (Cancelled)

19. (Original) A memory apparatus comprising:

a first memory chip;

a second memory chip; and

a designated terminal to be supplied an operation voltage,

wherein said first memory chip has a first terminal, a second terminal and a voltage circuit,

wherein said second memory chip has a third terminal,

wherein said designated terminal couples to said first terminal of said first memory chip and said third terminal of said second memory chip and is supplied an operation voltage,

wherein said second terminal of said first memory chip is supplied one of a first state signal and a second state signal according to a voltage level of said operation voltage,

wherein said second terminal is supplied said first state signal, said first memory chip is supplied a first voltage as said operation voltage and generates an internal operation voltage from said first voltage by said voltage circuit,

wherein said second terminal is supplied said second state signal, said first memory chip is supplied a second voltage as said operation voltage and generates said internal operation voltage from said second voltage by said voltage circuit, and

wherein said first voltage is lower voltage than said second voltage.

20. (Original) A memory apparatus according to claim 19,

wherein said voltage circuit comprises a charge pump including a plurality of stages,

wherein when said second terminal is supplied said first state signal, said voltage circuit uses a first stage of said charge pump,

wherein when said second terminal is supplied said second state signal, said voltage circuit uses a second stage of said charge pump, and

wherein a boost rate of said first stage is more than a boost rate of said second stage.

21. (Original) A memory apparatus according to claim 20, further comprising a fourth terminal,

wherein said fourth terminal is supplied a reference voltage,

wherein said second terminal is fixedly coupled to one of said operation voltage or said reference voltage as said first state signal, and

wherein said second terminal is fixedly coupled to another one of said operation voltage or said reference voltage as said second state signal.

22. (Original) A memory apparatus according to claim 21,

wherein said reference voltage is a ground level.

23. (Original) A memory apparatus according to claim 22,

wherein said first memory chip is a volatile memory, and

wherein said second memory chip is a nonvolatile memory.

24. (Original) A nonvolatile memory apparatus comprising:

a first semiconductor chip;

a nonvolatile memory chip; and

a designated terminal pair for being supplied an operation voltage,

wherein said first semiconductor chip has a first terminal pair coupled to said designated terminal pair,

wherein said nonvolatile memory chip has a voltage circuit, a second terminal pair coupled to said designated terminal pair and a third terminal for being supplied one of a first state signal and a second state signal according to a voltage level of said operation voltage,

wherein when said third terminal is supplied said first state signal, said nonvolatile memory chip is

supplied a first voltage as said operation voltage and generates an internal operation voltage from said first voltage by said voltage circuit,

wherein when said third terminal is supplied said second state signal, said nonvolatile memory chip is supplied a second voltage as said operation voltage and generates said internal operation voltage from said second voltage by said voltage circuit and,

wherein said first voltage is lower than said second voltage.

25. (Original) A nonvolatile memory apparatus according to claim 24,

wherein said nonvolatile memory has a nonvolatile memory array, and wherein said voltage circuit generates a program voltage for programming data to said nonvolatile memory array.

26. (Original) A nonvolatile memory apparatus according to claim 25,

wherein said voltage circuit further generates an erase voltage for erasing data stored in said nonvolatile memory array.

27. (Original) A nonvolatile memory apparatus according to claim 26,

wherein when said first semiconductor chip is only operable by said second voltage as said operation voltage, and said third terminal of said nonvolatile memory is fixedly supplied said second state signal.